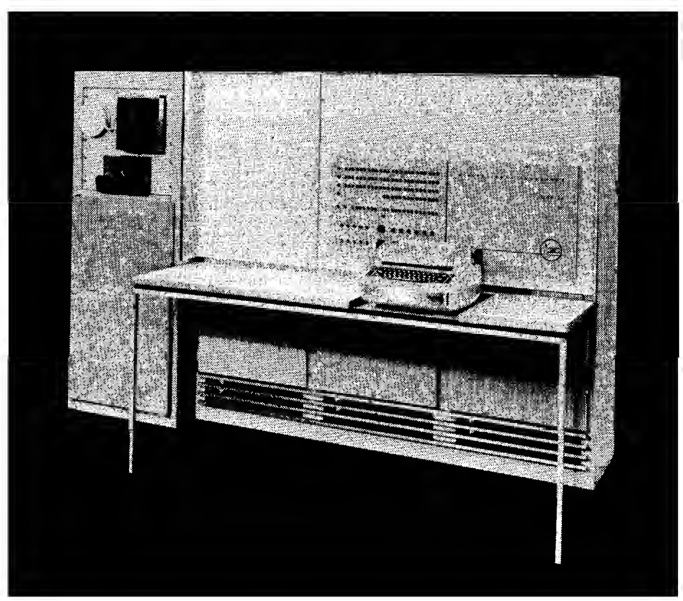
DDP-24



INTERFACE MANUAL

INTERFACE MANUAL
FOR THE
DDP-24
GENERAL PURPOSE COMPUTER

CONTENTS

DDP-24

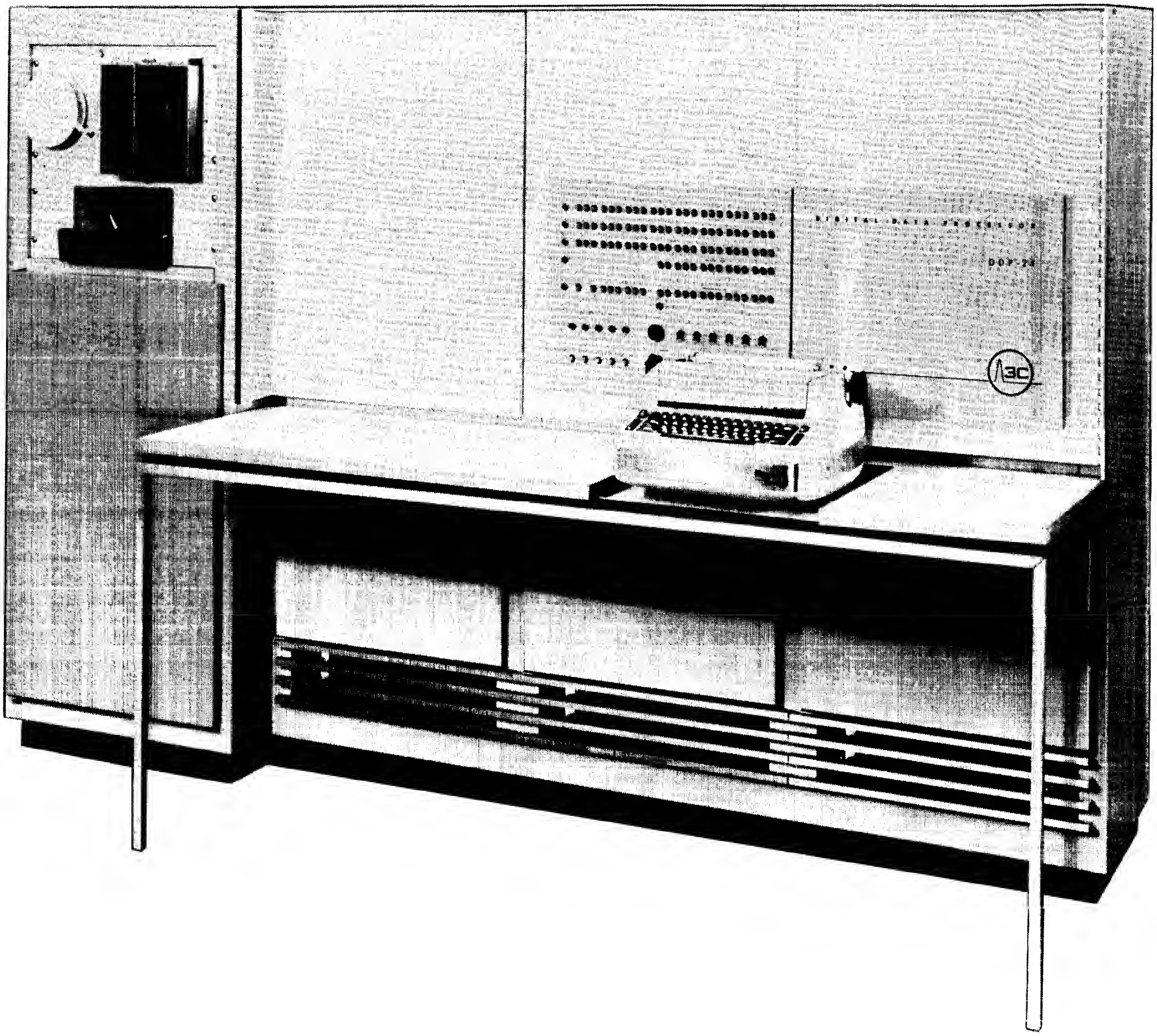


FIGURE 1—STANDARD DDP-24

INTRODUCTION

The DDP-24 General Purpose Computer (Figure 1) features strong input-output capabilities, particularly easy expandability by modular design, variety of input-output modes, and simplicity of operation. A general description of the input-output operation is given in the DDP-24 Reference Manual.

This manual is intended to show the interface characteristics of the DDP-24 to allow proper connection with peripheral equipment. Descriptions are given of the operation and signal characteristics of different input-output channels, sense lines, output control lines, interrupt lines, word-forming buffer, direct memory access, and fully buffered channels. Connectors and pin assignments are given.

All input-output logic consists of standard Computer Control Company S-PAC modules. The basic NAND gate circuit used is shown in Figure 2. Further information on the NAND gate and other S-PAC circuits used in the DDP-24 is given in the regular S-PAC manual.

All input signals are amplified by at least one NAND gate stage if used as dc levels and by at least two NAND gate stages if the leading or trailing edge transitions are used. All output signals from the DDP-24 are NAND gate outputs. In general, TRUE, SET, or ONE signals correspond to the —6 volt level; FALSE, RESET, or ZERO to 0 volt. Consequently, all pulses are negative-going except the output control pulse which is positive-going.

INPUT-OUTPUT CHANNELS

PARALLEL INPUT CHANNELS

Transfer of input data using a parallel input channel is illustrated by the block diagram of Figure 3. The internal logic shown has been slightly simplified for ease of explanation without affecting the characteristics of input and output signals. Data transfer of 24-bit words into the computer can take place under control of any of the DDP input commands INM, INA, or FMB

NOTE

Descriptions of command mnemonics are provided in the DDP-24 Reference Manual.

The input drop-in pulse sets the channel ready flip-flop with a positive transition. The channel ready signal is connected to the sense matrix, where it can be tested by the SKS instruction. This signal can also be connected to an interrupt line to initiate an interrupt if the input channel is connected to operate in that mode.

The channel ready signal is also available through a NAND gate to the input device as a channel busy signal. The channel enable flip-flop is set with the execution of a properly coded OCP command if not already set.

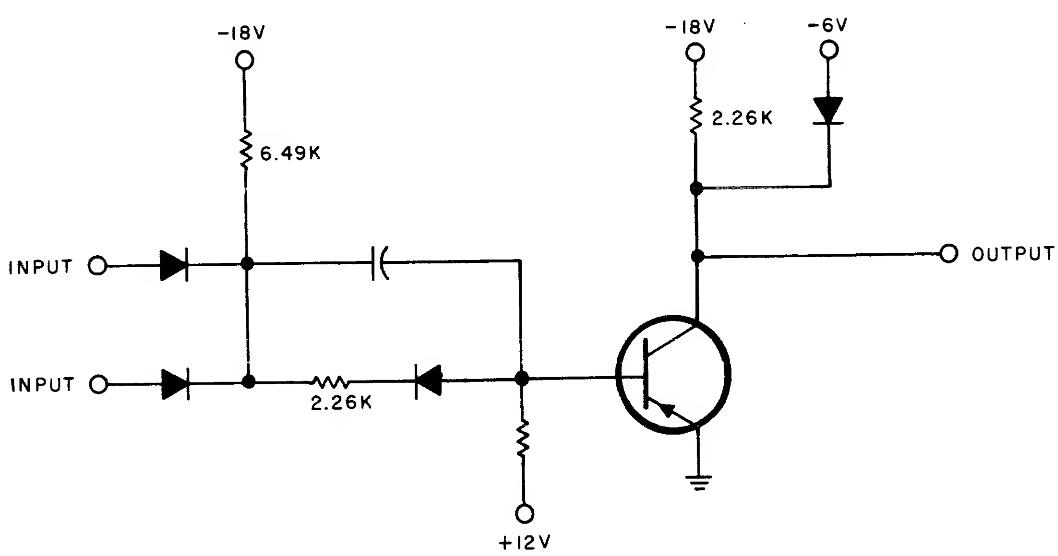


FIGURE 2—BASIC NAND GATE CIRCUIT

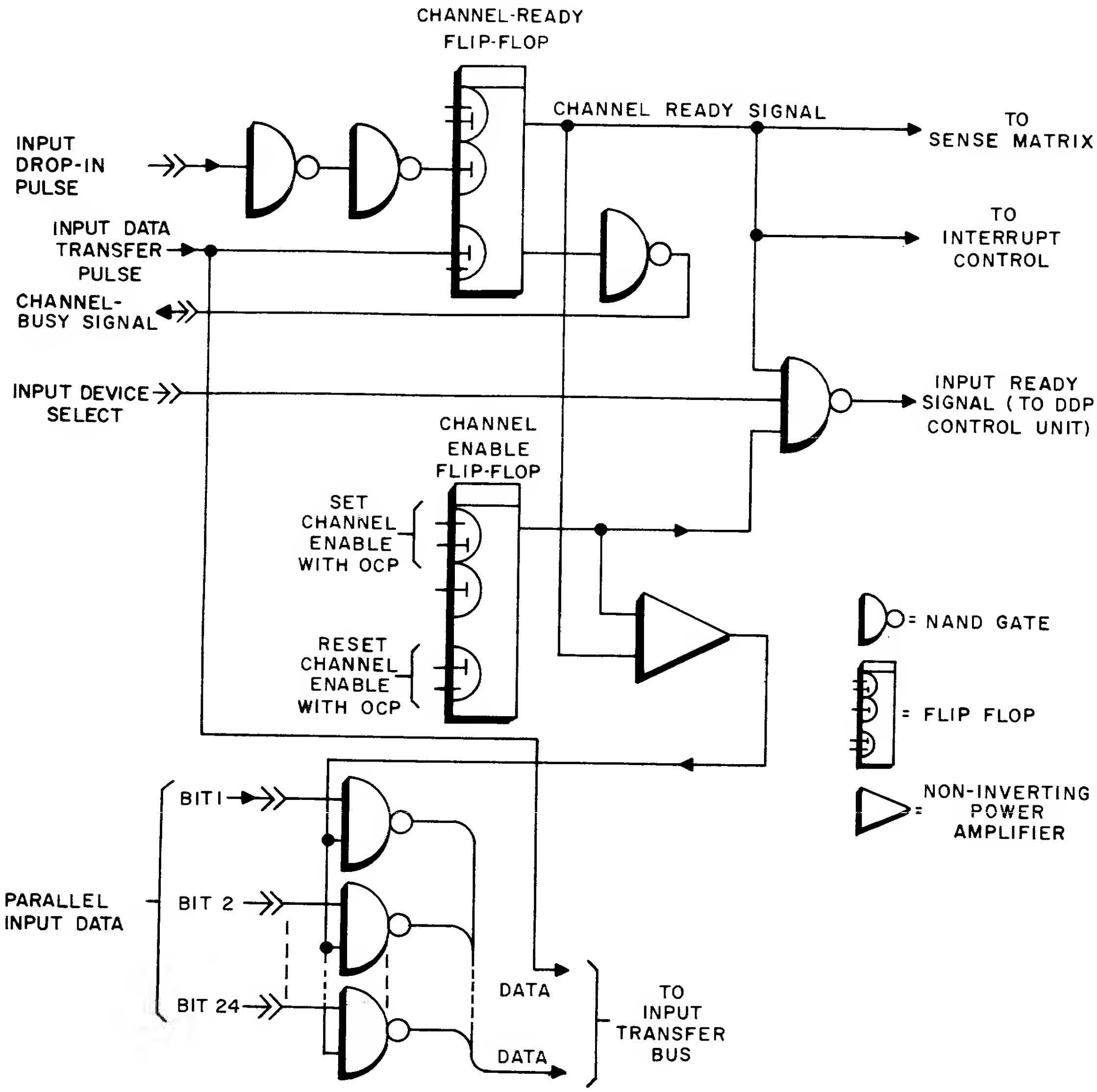


FIGURE 3—PARALLEL INPUT CHANNEL

An input device select signal may be provided by the input device, to be gated with the channel ready and channel enable signal. This corresponds to the input ready signal which enables the DDP input commands FMB, INA, INM. If no input device select signal is provided this open input acts as a TRUE signal.

The 24-bit parallel inputs are dc signals which must have attained their correct level not later than 3 μsec after the trailing edge of the input drop-in pulse. ONE level corresponds to —6 volts; ZERO level to 0 volt. The input data transfer pulse gates the 24-bit input data through the input transfer bus onto the DDP transfer bus after the channel ready and channel enable flip-flops have been set. The input data transfer pulse is a 1 μsec pulse generated during the execution of either FMB, INA, or INM commands. The input levels can be removed immediately after the trailing edge of the data transfer pulse.

SPECIFICATIONS OF THE SIGNALS TO AND FROM THE PARALLEL INPUT CHANNEL

INPUT DROP-IN PULSE:

TRUE level:	—5.5 volts to —6.5 volts
FALSE level:	0 volt to —1.5 volts
Pulse specifications:	5 μsec max rise time (90% to 10%); 0.6 μsec min width of the negative signal (measured from 90% point on the falling edge to the 90% point on the rising edge); 0.25 min. μsec width of applied logical ZERO (measured from 10% point on the rising edge to 10% point on the falling edge).
Input loading:	2.8 ma when driving source at 0 volt; 0 ma when driving source is at —6 volts.

CHANNEL BUSY SIGNAL:

ONE level:	—6 volts
ZERO level:	0 volt
Loading:	17 ma and up to 400 pf of stray capacitance
Rise time:	0.1 μsec (nom)
Fall time:	0.15 μsec (nom)

INPUT DEVICE SELECT:

TRUE level:	—5.5 volts to —6.5 volts
FALSE level:	0 volt to —1.5 volts
Input loading:	2.8 ma at 0 volt; 0 current at —6 volts.

PARALLEL INPUT DATA:

ONE level:	—5 volts to —6.5 volts
ZERO level:	0 volt to —1.5 volts
Input loading:	2.8 ma at 0 volt; 0 current at —6 volts.

The channel ready (and channel busy) signal is reset at the trailing edge of the input data transfer pulse. This completes the input cycle, and the input device can then remove the data signals from the input lines.

The channel enable flip-flop can be set at any time prior to the data transfer pulse. The data transfer pulse will be inhibited until the channel ready, channel enable, and input device select signals (if used) are set.

The timing of data inputs is illustrated in Figure 4, the timing chart for the parallel input channel. The positive transition of the input drop-in pulse sets the channel ready flip-flop; the negative transition may occur at any time, the only limitation being that it not be initiated before 0.25 μsec after completion of the positive transition and not later than 0.6 μsec before the next positive transition.

The rise time of the positive transition of the input drop-in pulse must be 5 μsec or faster. Input data are dc levels. Any level transition must be completed not later than 3 μsec after initiation of the positive transition of the input ready pulse.

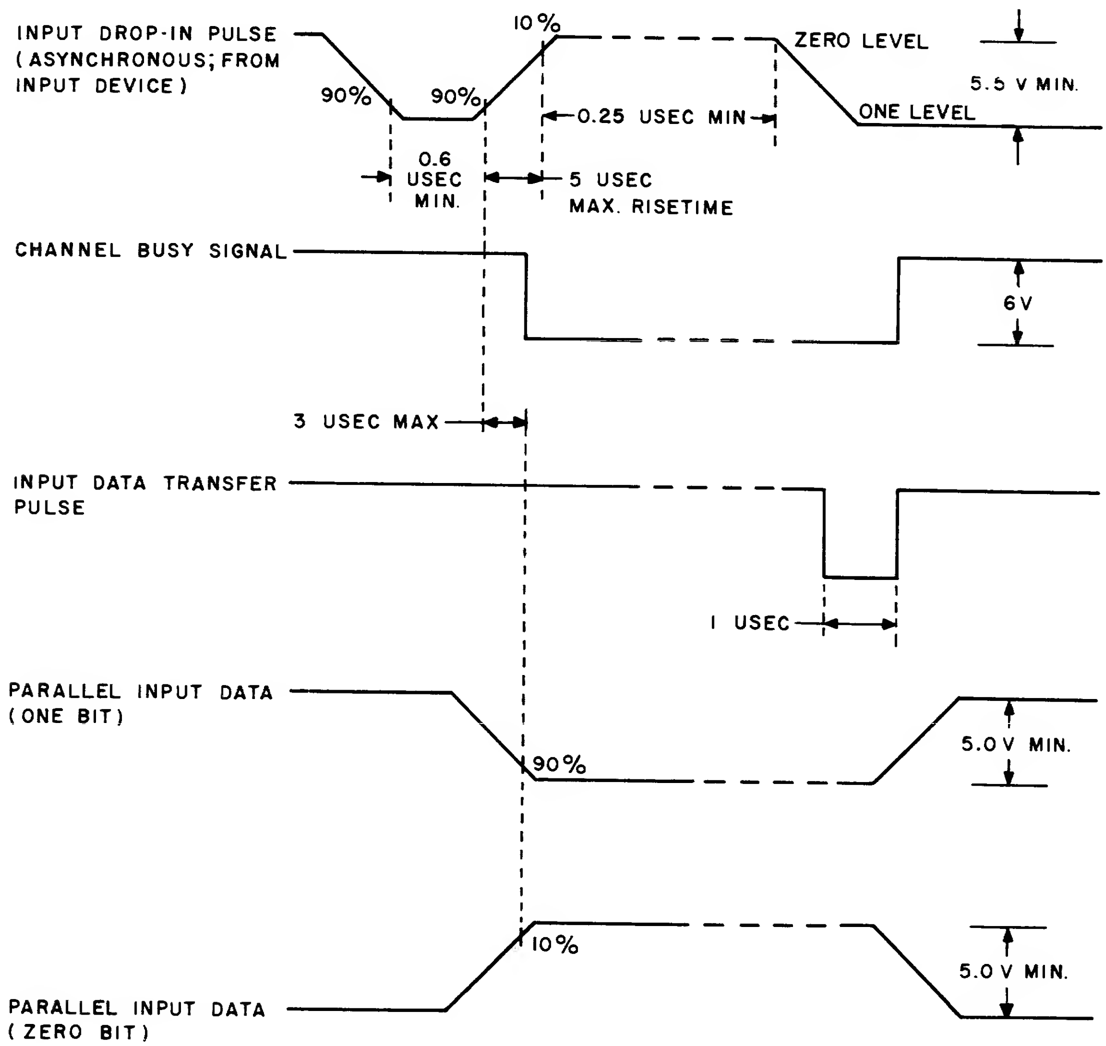


FIGURE 4—PARALLEL INPUT CHANNEL TIMING CHART

PARALLEL OUTPUT CHANNELS

The block diagram of the parallel output channel, Figure 5, shows the output of parallel data. It is similar to the parallel input channel.

The output device places an ac positive transition on the output busy line which, in turn, sets the channel ready flip-flop. The channel ready signal is used similarly as in the parallel input channel. It is connected to the sense matrix and to the interrupt control (if operating in interrupt mode). The channel ready signal is also available to the output device as a channel busy signal.

The channel enable flip-flop, if not already set, is set with the execution of an OCP command. An output device select signal sets the channel ready flip-flop when it changes to the TRUE level, the signal resets this flip-flop when it returns to the FALSE level (not shown in Figure 5.) This feature is specifically required if the output channel operates in the interrupt mode. The data transfer pulse is a 1 μsec pulse, which is generated during the execution of an output command (either DMB, OTA, or OTM) and gated with the channel ready, channel enable, and device select signals.

The output data transfer pulse is gated with the parallel bits from the output transfer bus. The output data therefrom consists of 1 μsec, positive-going pulses for ZERO bits, or −6 volt dc levels for ONE bits.

At the trailing edge of the output data transfer pulse, the channel ready flip-flop is reset, and the channel busy signal becomes false. (See Figure 6.) This action completes the output cycle.

The timing diagram for the parallel output channel, Figure 6, illustrates the timing relationships between the signals. After the output busy signal has enabled the setting of the channel ready flip-flop (and output channel busy signal) the output data pulses will take place at least 4 μsec later. This minimum interval will occur if the execution of the output command had been blocked by the reset channel ready signal.

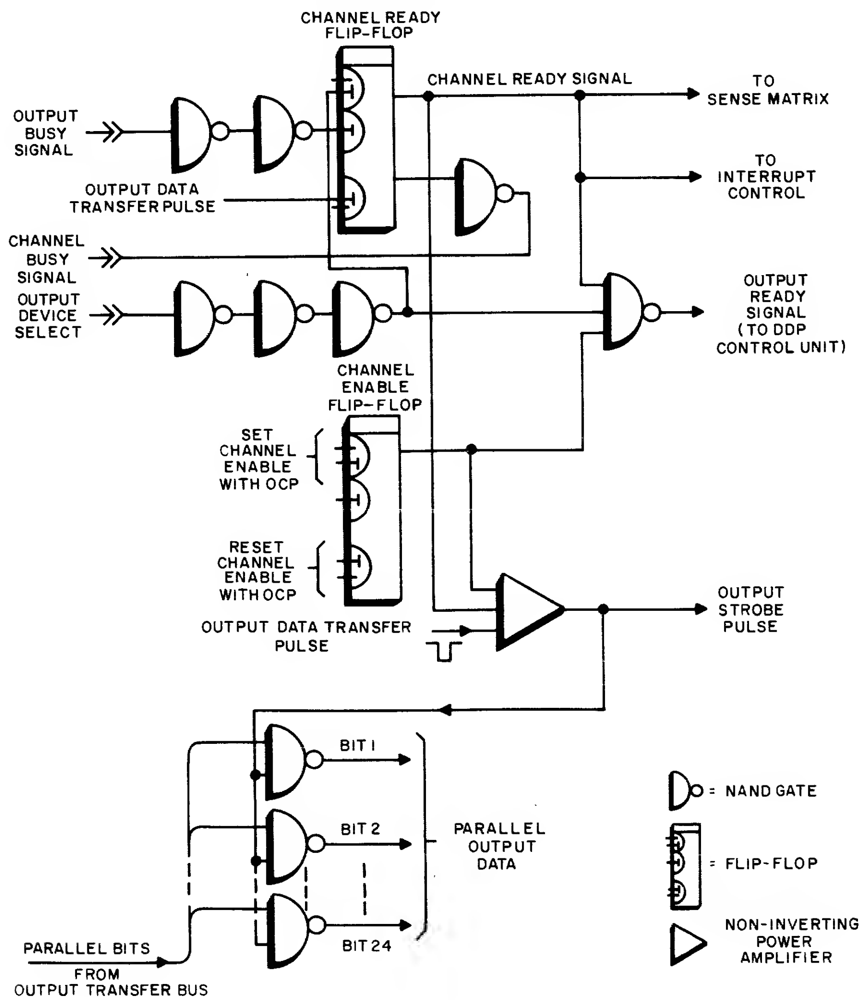


FIGURE 5—PARALLEL OUTPUT CHANNEL, BLOCK DIAGRAM

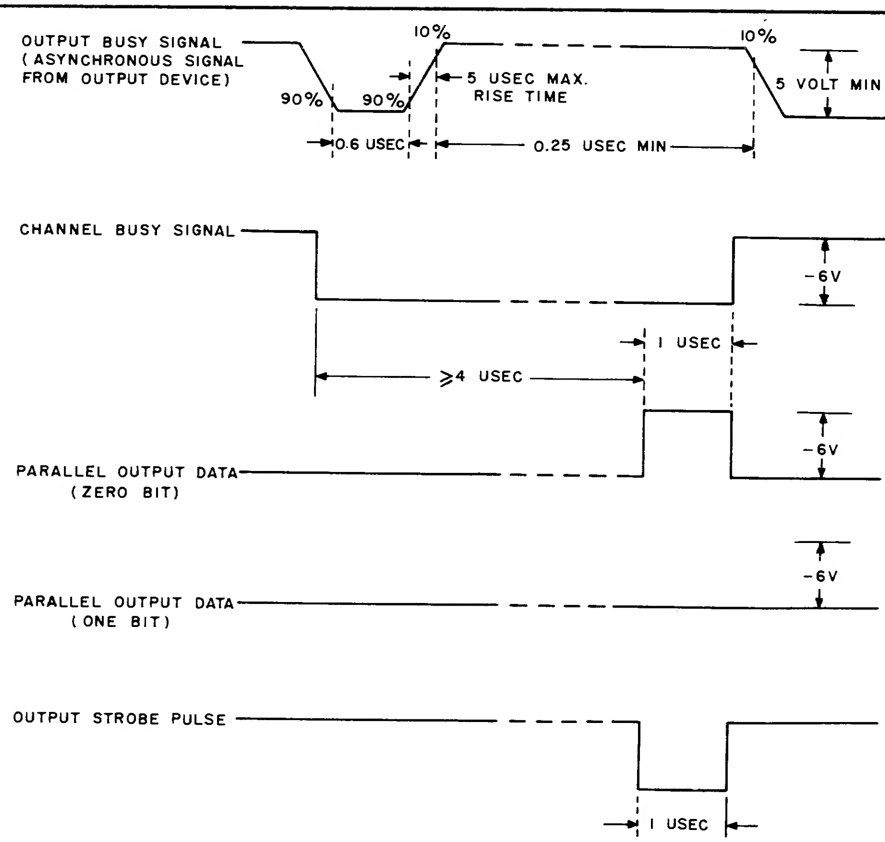


FIGURE 6—TIMING DIAGRAM FOR PARALLEL OUTPUT CHANNEL

SPECIFICATIONS SIGNAL PARALLEL OUTPUT CHANNEL

OUTPUT BUSY SIGNAL:

TRUE level:	—5.5 volts to —6.5 volts
FALSE level:	0 volt to —1.5 volts
Pulse specifications:	5 μsec, rise time (90% to 10%); at least 0.6 μsec width of the negative signal measured between 90% points on falling and rising edge; 0.25 μsec width of applied logical ZERO, measured between 10% points on rising and falling edge.
Input loading:	2.8 ma when driving source is at 0 volt; 0 current when driving source is at —6 volts.

OUTPUT CHANNEL BUSY:

ONE level:	—6 volts
ZERO level:	0 volt
Loading:	17 ma and up to 400 pf of stray capacitance
Rise time:	0.1 μsec (nom)
Fall time:	0.15 μsec (nom)

OUTPUT DEVICE SELECT:

TRUE level:	—5 volts to —6.5 volts
FALSE level:	0 volt to —1.5 volts
Rise time:	5 μsec max. (90% to 10%)
Input loading:	2.8 ma at 0 volt, 0 current at —6 volts.

OUTPUT STROBE:

ONE level:	—6 volts
ZERO level:	0 volt
Waveform width:	1 μsec
Rise time:	0.1 μsec (nom)
Fall time:	0.15 μsec (nom)
Loading:	40 ma and up to 1500 pf of stray capacitance

OUTPUT DATA:

ONE level:	—6 volts dc
ZERO level:	Positive pulse between —6 volts and 0 volt

OUTPUT WAVEFORM:

Rise time:	0.1 μsec (nom)
Fall time:	0.15 μsec (nom)
Width:	1 μsec
Output loading:	17 ma and up to 400 pf of stray capacitance.

BUFFERED INPUT-OUTPUT CHANNELS

Figure 7, the general block diagram of the buffered input-output channel, applies to either character buffers or optional buffered parallel channels for 24-bit input and/or output. The channel ready, channel enable, and buffer flip-flops and the input and output gates are shown. Several input-output devices may be connected to the buffer, but only one device per buffer may be operating at a time. The buffer may be used for input or output, but not for both simultaneously. The drop-in pulse (for the input devices) or the output busy pulse (for output devices) sets the channel ready flip-flop with an ac positive transition. For output devices the channel ready signal should be turned on only when the device itself has been properly selected and enabled.

The channel ready flip-flop is connected to the sense matrix, to the control unit of the DDP processor, and to the interrupt control (if wired in). The channel ready flip-flop output is also made available to the input-output device(s) as a channel busy signal.

The channel enable flip-flop is set by the execution of an OCP command if not already set; it is reset when another channel enable flip-flop is set.

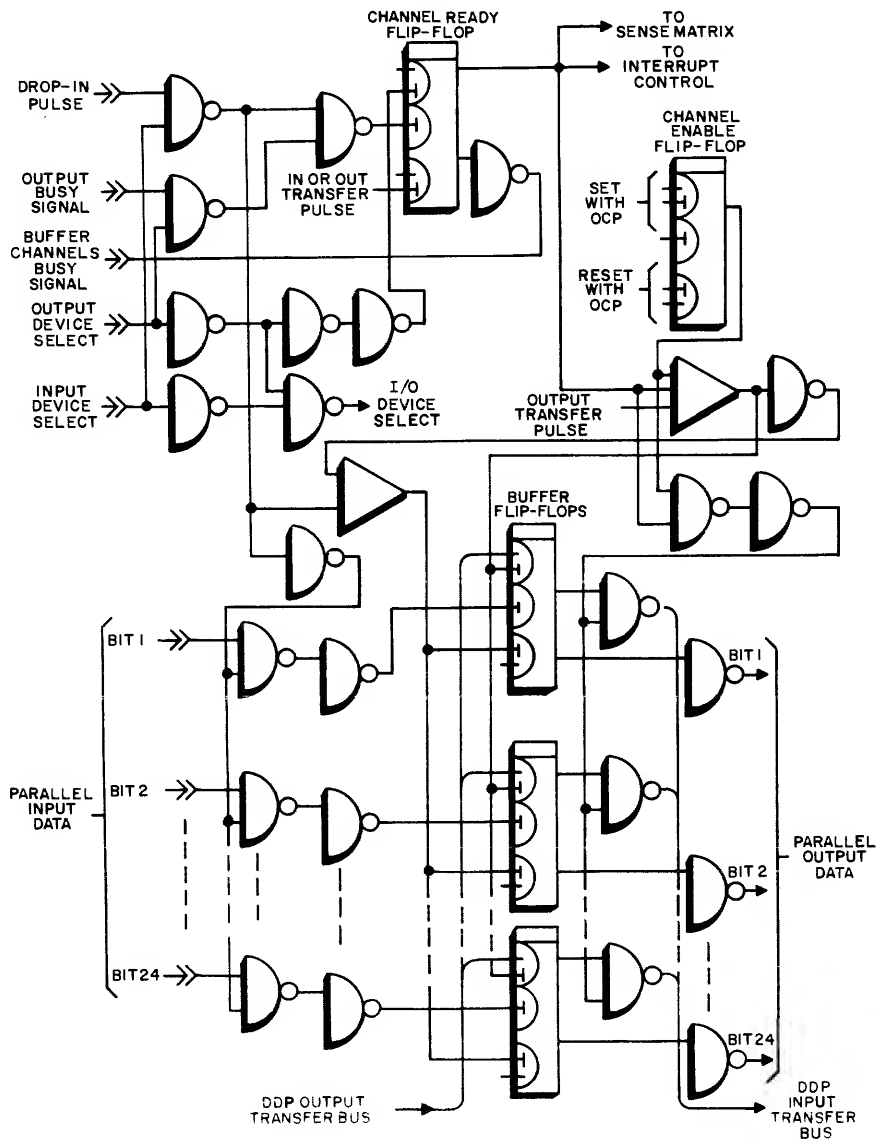


FIGURE 7—BUFFERED INPUT-OUTPUT CHANNEL, BLOCK DIAGRAM

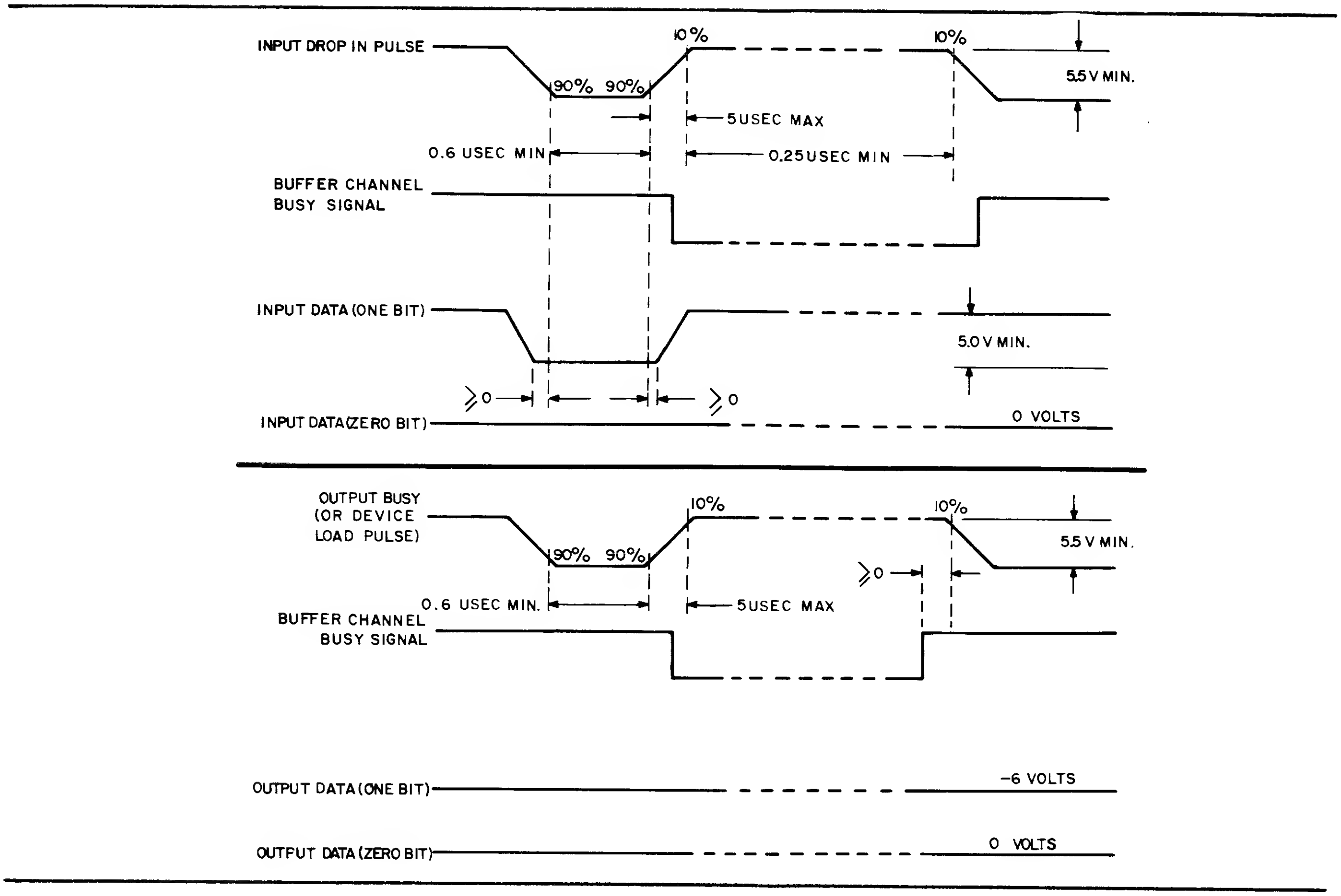


FIGURE 8—TIMING DIAGRAM FOR SIGNALS BETWEEN INPUT-OUTPUT DEVICES AND BUFFERED CHANNELS

The data transfer pulses for either input or output are generated as in the parallel input or output channels. They are gated with one of either the input or output commands.

The input data is gated with the input device drop-in pulse and, in turn, sets the flip-flop buffer with its positive transition trailing edge. Output data is read from the buffer flip-flops through NAND gates.

The channel ready flip-flop is reset with the positive transition (trailing edge) of either one of the data transfer pulses.

Only one device per buffer can be operating at one time. It is possible to select another device on a buffer and thereby switch off the one which had been selected before. To avoid losing any information that might have been stored in the buffer flip-flops, this switching off of an input-output device is to take place only under certain conditions. An output device can be switched off only when the channel ready flip-flop is set; an input device can be switched off when the channel ready flip-flop is reset (The channel ready flip-flop corresponds to the input-output channel busy signal.)

An interlock in the control logic for the standard input-output devices connected to the DDP-24 character buffer allows selecting and switching off of the devices only when permitted. The buffered channel ready flip-flop is reset when an output device is switched off (not shown in Figure 7) and is set when an output device is selected. In general, the channel ready flip-flop can be connected to the interrupt control of the DDP-24, but with more than one character device on a buffer it is also possible to connect proper signals from any of the devices to an interrupt line. This allows the operating of devices in both the ready and interrupt modes on the same channel. (But still only one device per channel can operate at a time.)

The timing diagram, Figure 8, shows waveforms and timing specifications of the signals between buffered channels and input-output devices. Signal characteristics are similar to those of the non-buffered input and output channels as follows.

SIGNAL SPECIFICATIONS NON-BUFFERED CHANNELS

INPUT DROP-IN AND OUTPUT BUSY SIGNAL:	
TRUE level:	−5.5 volts to −6.5 volts
FALSE level:	0 volt to −1.5 volts
Pulse specifications:	5 μsec max reset time; 0.6 μsec min width of negative signal; 0.25 μsec min width of ZERO level.
Input loading:	2.8 ma at 0 volt and 0 current at −6 volts
BUFFER CHANNELS BUSY SIGNALS:	
ONE level:	−6 volts
ZERO level:	0 volt
Loading:	17 ma and up to 400 pf of stray capacitance
Rise time:	0.1 μsec (nom)
Fall time:	0.15 μsec (nom)
INPUT DEVICE SELECT SIGNALS:	
TRUE level:	−5.5 volts to −6.5 volts
FALSE level:	0 volt to −1.5 volts
Input loading:	2.8 ma at 0 volt; 0 current at −6 volts.
INPUT DATA SIGNALS:	
ONE level:	−5 volts to −6.5 volts
ZERO level:	0 volt to −1.5 volts
Input loading:	2.8 ma at 0 volt; 0 current at −6 volts.
OUTPUT DEVICE SELECT SIGNALS:	
TRUE level:	−5 volts to −6.5 volts
FALSE level:	0 volt to −1.5 volts
Rise time:	5 μsec max (90% to 10%)
Input loading:	2.8 ma at 0 volt; 0 current at −6 volts.

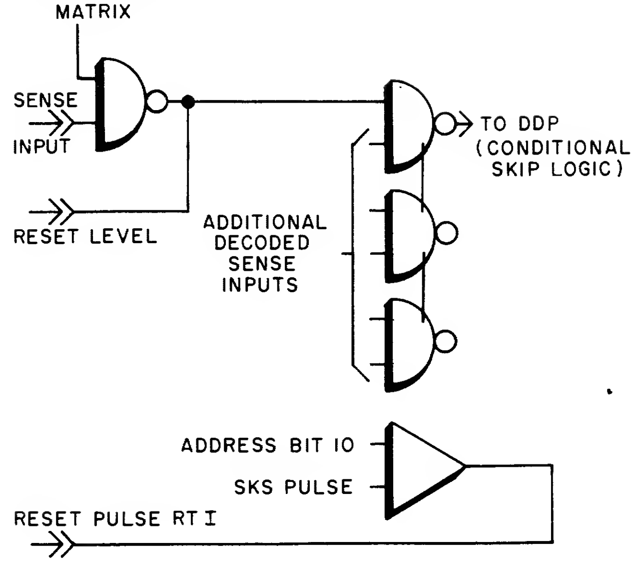


FIGURE 9—TYPICAL SENSE LINE INPUT

OUTPUT DATA SIGNALS:	
ONE level:	−6 volts dc
ZERO level:	0 volt
Output loading:	17 ma and up to 400 pf of stray capacitance.

In the character buffer, input-output data transfer takes place for six bits only. In addition, the character buffer provides odd parity detection for input characters, odd parity generation for output characters; it also provides stop code detection and generation. The characteristics of the single-bit parity signals and stop code signals for input or output are identical to those of the data bits.

SENSE LINES

The DDP-24 includes a number of sense lines, which can be tested with the SKS (skip-if-sense-line-not-set) instruction. Sense lines provided as standard equipment on the DDP-24 include; 1) those from the ready flip-flops of the standard input-output channels; 2) from the sense switches on the control panel; 3) from certain internal flip-flops (such as overflow, improper divide, etc.) and 4) sixteen general purpose sense lines. Over 8000 sense lines can optionally be added. Optional equipment, such as from ready flip-flops of additional input-output channels, which requires sense line inputs to the computer, generally includes those sense lines with the option.

The standard and optional general purpose sense lines are tested with an SKS instruction according to its decoded address portion, and then bits 10 through 24. A 2 μsec select signal selects the sense line, then a 1 μsec test pulse steps the program counter if the sense input is not true. If bit 10 is ONE the test pulse is returned as a reset signal upon execution of the SKS instruction. This can reset the test signal.

For the proper decoding of the address portion of SKS, octave decoding is used. A decoding matrix of five octaves with eight decoders per octave is an integral part of the DDP-24. This matrix ensures simple and straightforward expansion.

The 16 general purpose sense lines that are standard with the DDP-24 correspond to octal address portion codes 20000 through 20007 and 30000 through 30007 (60000 through 60007 and 70000 through 70007 if reset). A general diagram for one sense line input is shown in Figure 9. SKS signal characteristics are shown in Figure 10.

SKS SIGNAL SPECIFICATIONS

SENSE INPUT SIGNALS:	
SET level:	−5 volts to −6.5 volts
NOT SET level:	0 volt to −1.5 volts
Input loading:	2.8 ma at 0 volt; 0 current at −6 volts.
RESET PULSE RTI:	
ONE level:	−6 volts
ZERO level:	0 volt
Output waveform width:	1 μsec
Rise time:	0.1 μsec (nom)
Fall time:	0.15 μsec (nom)
Output loading:	100 ma and up to 2000 pf of stray capacitance.

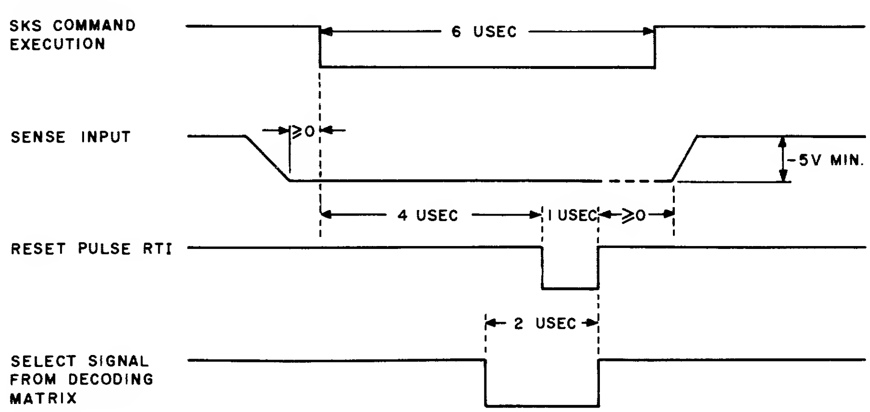


FIGURE 10—SKS SIGNAL CHARACTERISTICS

OUTPUT CONTROL CHANNELS

The output control pulse (OCP) instruction generates a 2 μsec pulse whose destination is controlled by the address portion, bits 10-15. The standard DDP includes certain OCP lines such as channel enable pulses for internal use. In addition, eight general purpose OCP lines are provided for external use. This number may optionally be expanded with either OCP pulse lines, output control dc signal lines, or output control dc signal lines with power drivers. OCP lines required as part of optional equipment generally are included with that equipment.

The address portion decoding of the OCP command makes use of the same integral decoding matrix as SKS. The eight standard OCP lines of the DDP-24 correspond to octal address portion codes 01010 through 01017. Figure 11 shows a simplified diagram of the different types of OCP lines. Figure 12 shows the timing of the output control pulse.

OCP SIGNAL SPECIFICATIONS

OUTPUT CONTROL PULSE:	
Polarity:	Positive going, between −6 volts and 0 volt
Width:	2 μsec
Rise time:	0.1 μsec (nom)
Fall time:	0.15 μsec (nom)
Output loading:	17 ma and up to 400 pf of stray capacitance.
OUTPUT CONTROL DC SIGNAL:	
TRUE level:	−6 volts
FALSE level:	0 volt
Output loading:	17 ma and up to 400 pf of stray capacitance.
OUTPUT CONTROL DC SIGNAL WITH POWER AMPLIFIER:	
TRUE level:	−6 volts
FALSE level:	0 volt
Output loading:	100 ma and up to 2000 pf of stray capacitance.

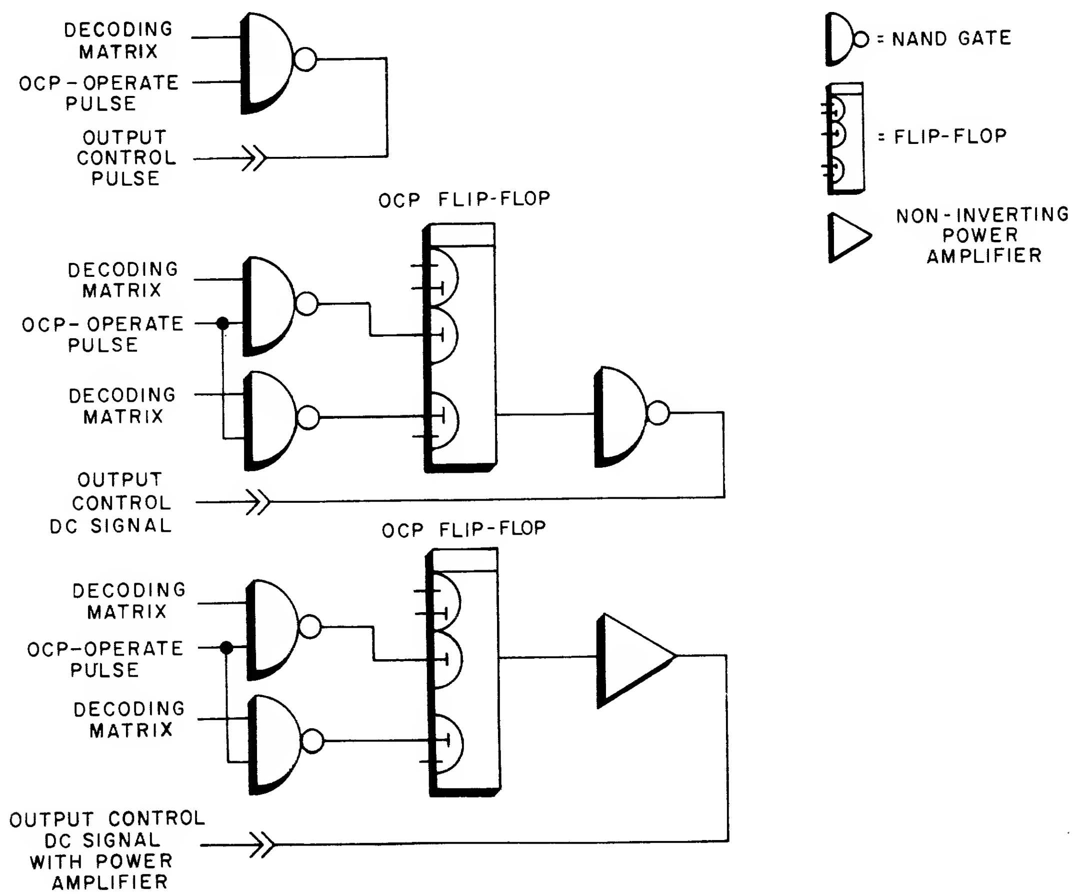


FIGURE 11—OUTPUT CONTROL PULSE LINES, BLOCK DIAGRAM

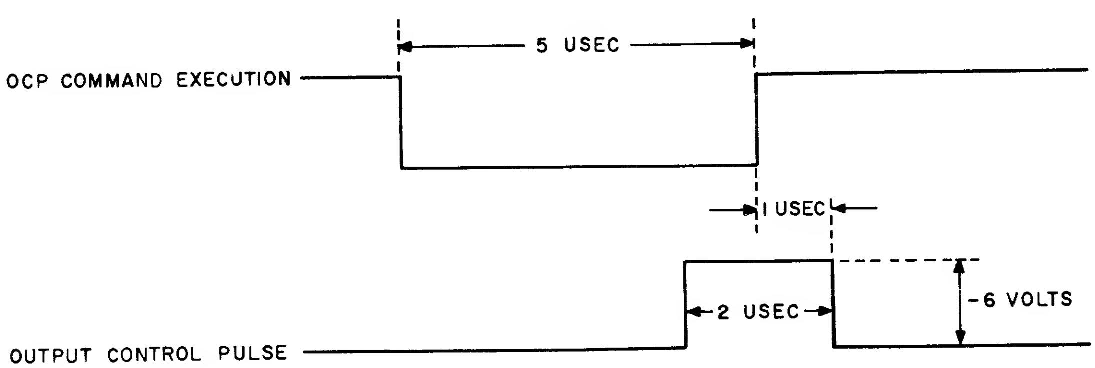


FIGURE 12—TIMING DIAGRAM OF OUTPUT CONTROL PULSES

INTERRUPT LINES

Four interrupt lines are standard with the DDP-24. This number can optionally be expanded to 32. A TRUE dc signal on an interrupt line will cause an interrupt of the computer program if the interrupt enable flip-flop is set. Upon completion of any current DDP-24 command, a program jump is made to an interrupt destination which is unique to the interrupt line. The contents of the program counter, the coded number of any enabled input-output channel, and the state of certain internal flip-flops are stored in memory.

During interrupt subroutines no further interrupts can be made. Therefore, upon return from an interrupt subroutine several new interrupt requests may have accumulated. A lockout or priority-on-stacking feature is provided in the standard DDP-24 so that only one interrupt line will cause a new interrupt. The priority-on-stacking is set up according to a preassigned priority, rather than a priority in order of occurrence. The interrupt request signals on the interrupt signal must be dc levels lasting at least until they are honored.

Four interrupt lines—L_0, L_1, L_2, and L_3—are standard with the DDP-24 with respective interrupt destinations 00001, 00003, 00005, 00007. The program counter contents and other information are automatically stored at 00000, 00002, 00004, and 00006, respectively. Interrupt line L_0 has the highest interlock priority; next highest is L_1, then L_2, then L_3.

Any proper dc signal can be connected to an interrupt line. Typical possible connections are: power failure detection, input-output channel ready flip-flops, overflow, improper divide, and parity flip-flops. Figure 13 shows the basic gating for the interrupt inputs. The interrupt input signal must be on for at least the time that it takes to start the interrupt subroutine, plus 3 μsec.

The interrupt routine must be terminated with a JRT command. This will not only restore the program counter to the location following the point of interrupt, but will also restore the channel enable and the other internal flip-flops as well as reset the interrupt flip-flop. The interrupt signal that caused the interrupt should be turned off by the end of the interrupt routine. Channel ready flip-flops that may cause interrupts are reset with the input or output command (either INA, INM, FMB, or OTA, OTM, DMB). Signals that are also connected to sense lines generally can be reset with the SKS command.

INTERRUPT SIGNAL SPECIFICATIONS

TRUE level:	−5.5 volts to −6.5 volts
FALSE level:	0 volt to −1.5 volts
Waveform:	3 μsec max rise and fall time (between 10% and 90%)
Input loading:	2.8 ma at 0 volt; 0 current at −6 volts.

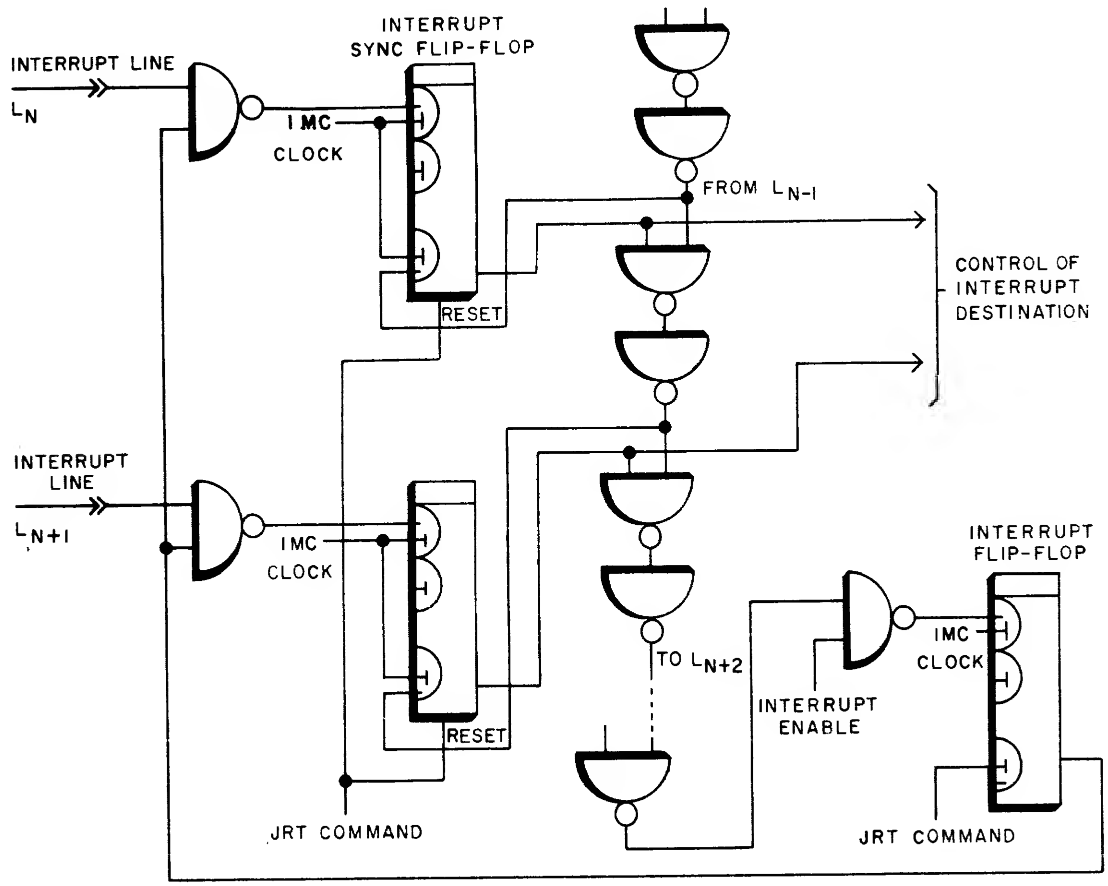


FIGURE 13—INTERRUPT LINES, BLOCK DIAGRAM

OPTIONAL INTERFACE EQUIPMENT

FULLY BUFFERED CHANNEL

The fully buffered channel (Figure 14) permits an external input-output device to communicate directly with up to two 4096-word memory modules for transfers of data at very high speed. Once set up and enabled by the computer program the address of the sequential memory locations to be accessed is supplied by the FBC independent of the computer program. In case the fully buffered channel and the computer program both address the same memory module, the fully buffered channel operates in a direct memory access mode (memory cycle stealing) as described below.

The maximum transfer rate of the channel is 166 kc. When the channel operates in a DMA mode the computer program will be fully interrupted for rates higher than 83 kc. The FBC consists of a 24-bit data register for buffering of input-output data, a 14-bit address register controlling addressing of the memory, a 13-bit range register providing a limit to the block transfer, operational mode flip-flop, and the FBC clock. Included are various control circuits, some of which are used internally to the FBC and others used in the coupling of the FBC to the external device. The FBC is set up initially by the DDP-24 by way of a regular parallel output channel that can be either the standard or any optional parallel output channel. This channel is not included within the FBC proper.

Under program control, a parallel output channel for address and range setup is first enabled with an OCP command. The computer program then loads the FBC address register and operational mode flip-flop with an OTM command. (Bit 1, the signbit of this OTM word, specifies input mode of operation if ZERO, and output mode if ONE.) The range register is then loaded with a second OTM instruction. When bit 2 (the bit next to the sign) of the first OTM word transferred by the computer program is ONE, the second OTM is not necessary, and the range register will be loaded with all ONEs. The start address is 14 bits, and the range register is 13 bits. Therefore the FBC can address up to 8192 memory cells starting with the initial address in the FBC address register. (Variations of the regular FBC allow addressing 12,288 and 16, 384 memory cells.)

NOTE

The FBC will address memory modules sequentially and does not have a wrap-around capability.

The FBC address register is incremented with a ONE and the range register is decremented with a ONE after a memory read or write cycle is initiated. When the total number of words specified in the range register has been transferred from or to the FBC, the channel will be disabled, and no further words will be transferred. Any memory location within the two 4096-word memory modules addressable by the regular FBC can be the start address and the stop address for the block transfer. The start address must always be in a lower memory location. The FBC can be disabled with an external stop signal. A power failure in the DDP system will also disable the fully buffered channel.

Eight control lines are used between the FBC channel and the external device. A short description of each is provided below.

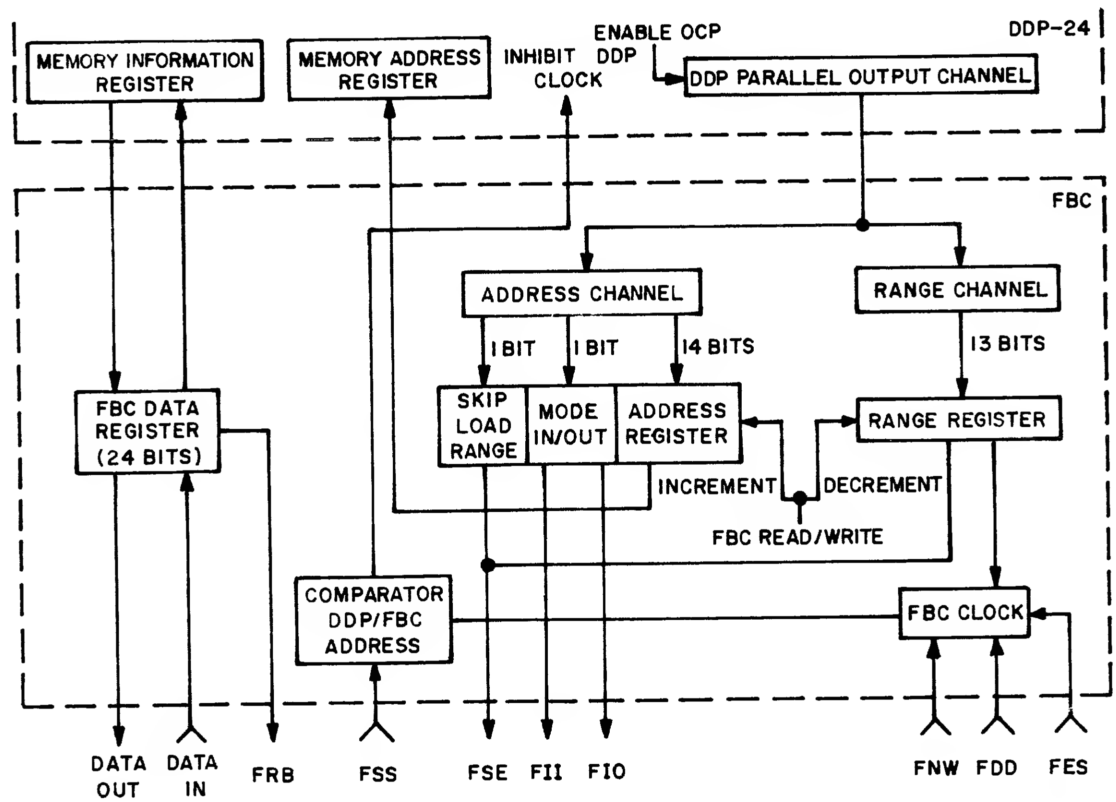


FIGURE 14—FULLY BUFFERED CHANNEL, BLOCK DIAGRAM

FSE This is the FBC start enable pulse generated by the FBC after the address and range registers have been properly loaded. Its trailing edge can be used to start a device. Signal specifications: negative-going, NAND gate output pulse between —6 volts and 0 volt; 1 μsec wide; rise time of 0.1 μsec (nom); fall time of 0.15 μsec (nom); output loading of 17 ma; and stray capacitance of 400 pf.

FII A flip-flop level indicating that the FBC is in the input mode if TRUE (reading from the external device to the memory). The FII flip-flop is set when the range and address registers have been loaded if the sign bit of the first OTM word was a ZERO. The FII flip-flop is reset by a stop signal from the external device, by a power failure interrupt of the DDP-24, or upon reading the number of words specified by the range register. Signal specifications: negative-going, NAND gate output pulse with TRUE level of —6 volts and FALSE level of 0 volt; output loading of 17 ma; and stray capacitance of 400 pf.

FIO A flip-flop level indicating that the FBC is in the output mode if TRUE. The FIO flip-flop is set after the address and range registers have been loaded if the sign bit of the first OTM word was a ONE. It is reset by a stop signal from the external device, by a power failure interrupt of the DDP-24, or upon reading the number of words specified by the range register. Signal specifications are the same as for FII.

FRB This is the FBC data register busy flip-flop which is set in the output mode when the FBC initiates a read memory cycle, and in the input mode when the buffer register contains a new word from the external device. It is reset in the output mode as soon as the buffer register has been refilled with information or in the input mode after the contents of the FBC register have been transferred into the memory. Signal specifications are the same as FII.

FNW The read-next-word pulse from a device during the output mode. Its trailing edge sets the FBC demand flip-flop. Signal specifications: negative-going pulse with TRUE level of —5.5 volts to —6.5 volts and FALSE level of 0 volt to —1.5 volts; 0.6 μsec minimum width and 3 μsec maximum width of the TRUE signal (between 90% points); 4 μsec minimum width of the FALSE signal (between 10% points); maximum rise and fall time of 5 μsec (between 10% and 90% points); input loading of 2.8 ma at 0 volt; and 0 current at —6 volts.

FDD The drop-in pulse from a device during the input mode. It sets the FBC demand flip-flop and FRB flip-flop after information has been transferred into the FBC data register. FDD is a negative-going pulse with the same signal specifications as the FNW. In addition the drop-in pulse cannot be any wider than 1/5 of the cycle, in μsec, at maximum operate speed of the external device.

FES The external stop signal given by a device that resets FIO or FII thereby disabling the FBC data channel and preventing any further data transfer. FES is a negative-going pulse with the same signal specifications as the FNW and FDD signals.

FSS A pulse generated by an input-output device during the fast input mode (speed of device greater than 83 kc) the trailing edge of which occurs at least 7 μsec before the first drop-in pulse. (Any delay greater than 7 μsec can interrupt the computer for the same amount of time.) This pulse enables a comparison circuit that checks that the FBC is in a DMA mode and ensures that the first word from the device will be transferred. FSS is a negative-going pulse with the same signal specifications as the FNW.

The FBC interrogates the address information contained in the program counter and in the effective address of the computer and inhibits the computer clock if both the FBC and the computer try to access the same memory module at the same time. The FBC operates then as in a direct memory access (DMA) mode. The computer clock will be inhibited if an operand access is to be processed or before an instruction is fetched while the FBC seeks access to the same memory module. The inhibit signal will be released after the FBC completes its memory access. The FBC in the DMA mode does not lock out the DDP during the performance of that portion of a long operation cycle that does not require a memory access. A fast and a slow mode of operation are possible for the FBC in the DMA mode under the control of a jumper wire. The fast mode is required if transfer rates higher than 83 kc occur. During the fast mode of operation with transfer rates between 83 and 166 kc, the computer will not be able to gain access to the FBC memory module for 12 μsec after the last FBC demand, in which case the program will be fully interrupted. In the slow mode of operation (less than 83 kc) the computer program will only be inhibited for 5 μsec (FBC memory access).

The DDP program counter and effective address are compared for at least 10 μsec before the FBC address approaches the first location in the next sequential memory module. If the DDP tries to gain access to the module that the FBC will address, the computer clock will be fully interrupted for up to 10 μsec, and after this time the FBC will be in a DMA mode.

Any of the dc level signals may be tested by the computer with the SKS instruction using a regular sense line. (Sense lines not included with the FBC.)

If an interrupt occurs in the computer program after processing the first OTM or the initial OCP during setup of the FBC, the parallel output channel of the computer will be disabled. The FBC will wait until the interrupt is completed and the channel has been returned to the enabled state. After the initial setup, an interrupt has no effect on the FBC.

DIRECT MEMORY ACCESS CHANNEL

The direct memory access (Figure 15) channel operates in the same way as the FBC when it addresses the same memory module as the DDP-24 program. The DMA channel always has priority access to memory over the DDP-24; but any current memory access by the computer, whether for command fetch or operand access, must be completed first. While the DMA has access to memory, the DDP is inhibited if it requires memory access. This is independent of any different memory module addressing by DMA and DDP.

Two operation modes are possible for DMA under control of a jumper wire: 1) a fast mode for data transfer rates of more than 83 kc in which each DMA memory access will inhibit DDP memory access for 12 μsec; 2) A slow mode for data transfer rates below 83 kc in which each DMA memory access inhibits DDP memory operation for only 5 μsec.

The DMA channel is to be set up with address and range information exactly as the FBC. It contains a 24-bit buffered data register, 14-bit address register, 13-bit range register, operational mode flip-flop, and DMA clock. The DMA can address any of the 16,384 memory locations, and transfers of up to 8192 word blocks are possible. As with the FBC, no wraparound addressing is possible, except when 16,384 memory locations may be addressed. The control lines between DMA and the external device are quite similar to signals of the fully buffered channel as follows.

DSE DMA start enable pulse.
Signal specifications same as for FSE.

DII DMA input mode level.
Signal specifications same as for FII.

DIO DMA output mode level.
Signal specifications same as for FIO.

DRB DMA register busy level.
Signal specifications same as for FRB.

DNW DMA read next word pulse.
Signal specifications same as for FNW.

DDD DMA drop-in pulse.
Signal specifications same as for FDD.

DES DMA external stop pulse.
Signal specifications same as for FES.

DSS DMA fast mode alert pulse.
Signal specifications same as for FSS.

WORD-FORMING BUFFER

The word-forming buffer (WFB) can operate in an input mode and in an output mode. In the input mode the WFM will form a 24-bit word from 6 bit characters received from an input device. In the output mode it will provide 6-bit characters from a 24-bit word to an

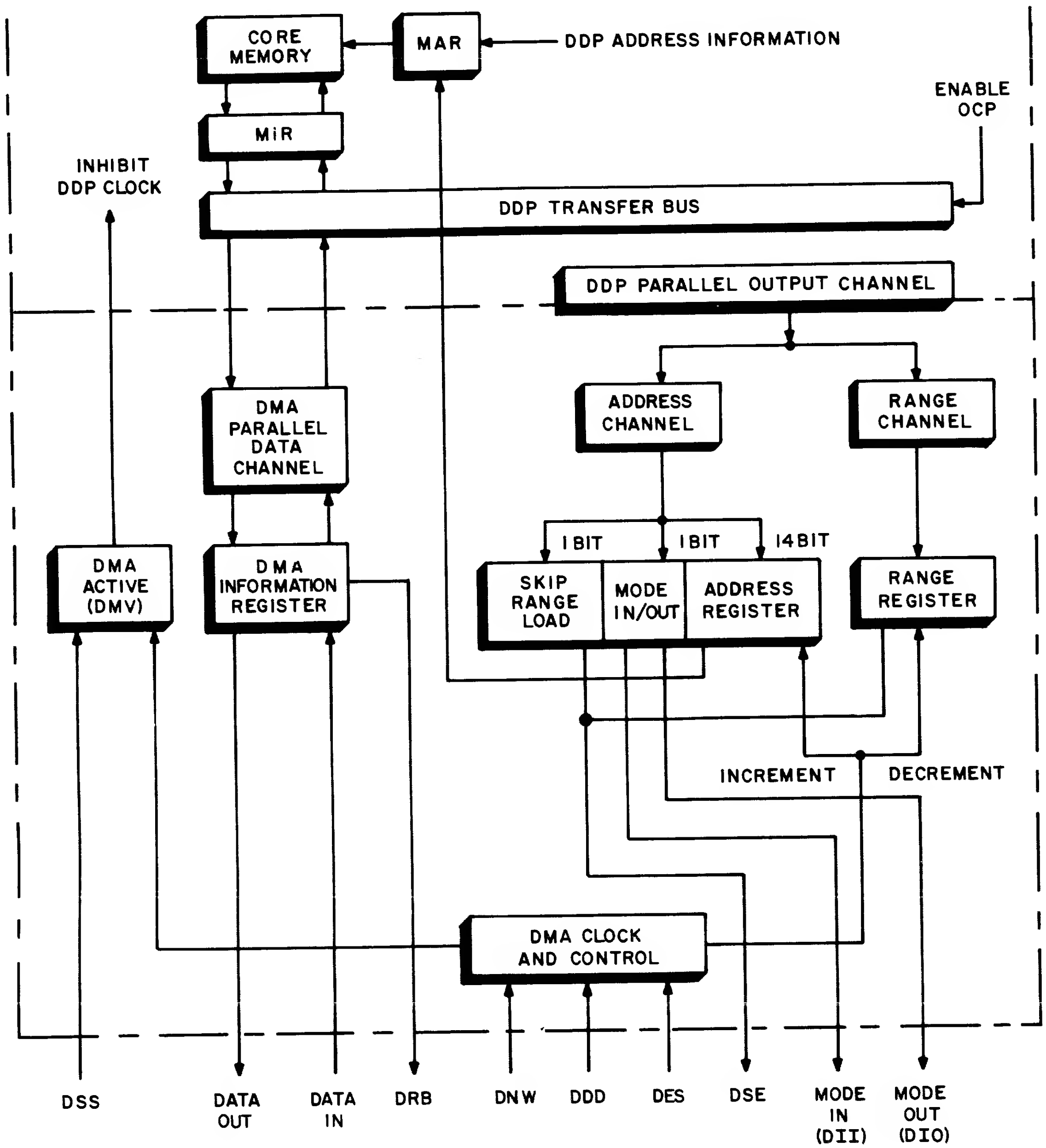


FIGURE 15—DIRECT MEMORY ACCESS CHANNEL, BLOCK DIAGRAM

output device. Odd parity checking and generating is provided. The word being formed or separated may consist of two, three, or four six-bit characters under control of OCP commands. When operated in a mode with fewer than four characters per word (i.e. two or three). The 12 or 18 least significant bits of the DDP word are filled or emptied. Parity may be disabled with an OCP command if desired.

SIGNALS USED IN THE INTERFACE BETWEEN THE WFB AND INPUT-OUTPUT DEVICE

INPUT DROP-IN AND OUTPUT BUSY SIGNAL:

TRUE level:	−5.5 volts to −6.5 volts
FALSE level:	0 volt to −1.5 volts
Pulse specifications:	5 μsec max reset time; 0.6 μsec min width of negative signal; 0.25 μsec min width of ZERO level.
Input loading:	2.8 ma at 0 volt; 0 current at −6 volts.

LAST CHARACTER SIGNAL:
(TRUE—when the last character is on the output data channel.)

TRUE level:	0 volt to −1.5 volts
FALSE level:	−5.5 volts to −6.5 volts
Loading:	17 ma and up to 400 pf of stray capacitance.

PARITY DISABLE SIGNAL:
(When TRUE setting of the parity flip-flop is inhibited)

TRUE level:	−5.5 volts to −6.5 volts
FALSE level:	0 volt to −1.5 volts
Input loading:	2.8 ma at 0 volt; 0 current at −6 volts.

INPUT DATA SIGNALS:

ONE level:	−5 volts to −6.5 volts
ZERO level:	0 volt to −1.5 volts
Input loading:	2.8 ma at 0 volt; 0 current at −6 volts.

OUTPUT DATA SIGNALS:

ONE level:	−6 volts dc
ZERO level:	0 volt
Output loading:	17 ma, and up to 400 pf of stray capacitance.

Note

The word-forming buffer may be attached to the optional DMA Channel or to a 24-bit parallel input-output channel.

CONNECTOR ASSIGNMENTS

CONNECTOR LAYOUT

The DDP-24 is equipped with a comprehensive connector panel at the rear of bay 4 of the cabinet. Figure 16 shows a rear view of the DDP-24 cabinet with the location of the connector panel. Figure 17 shows the connector panel itself. Besides the 6 connectors associated with the standard DDP up to 15 additional connectors may be used for optional input-output signals. All necessary connector cutouts are provided with the standard computer. More connectors can be accommodated if required by adding a connector panel at the rear bottom of bay 3.

One type of 50-pin connector is used on the connector panel: Cannon KOA2-21-L-50S. Mating plugs are provided with each DDP system. Plugs are: Cannon KOA3-21-50P, with KA5-21-5/8 shell. (See Figure 18 for polarization)

Tables 1 and 2 show the designation of all standard DDP-24 connectors, both those internally used as well as those on the connector panel. Tables 3 through 8 provide the pin functions of the connectors for the various channels.

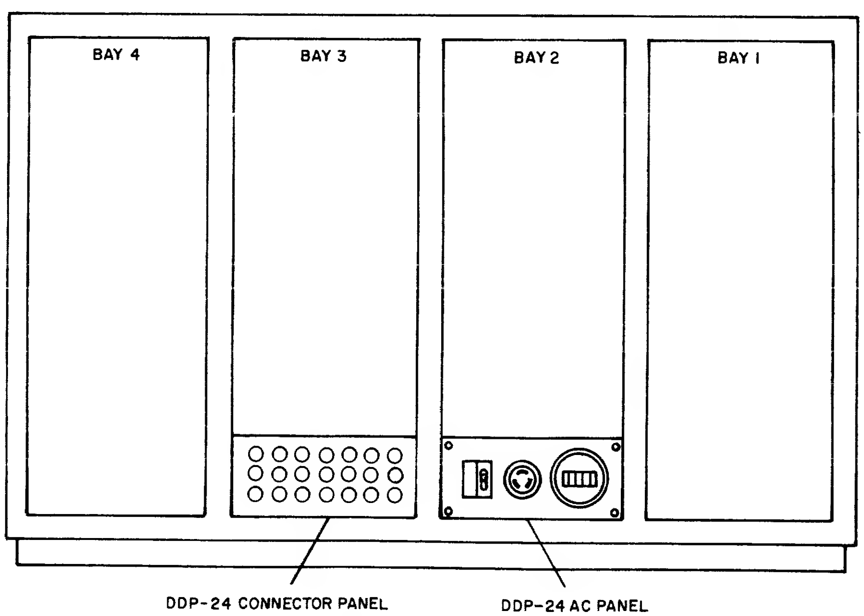


FIGURE 16—DDP-24, REAR VIEW, PANEL LOCATIONS

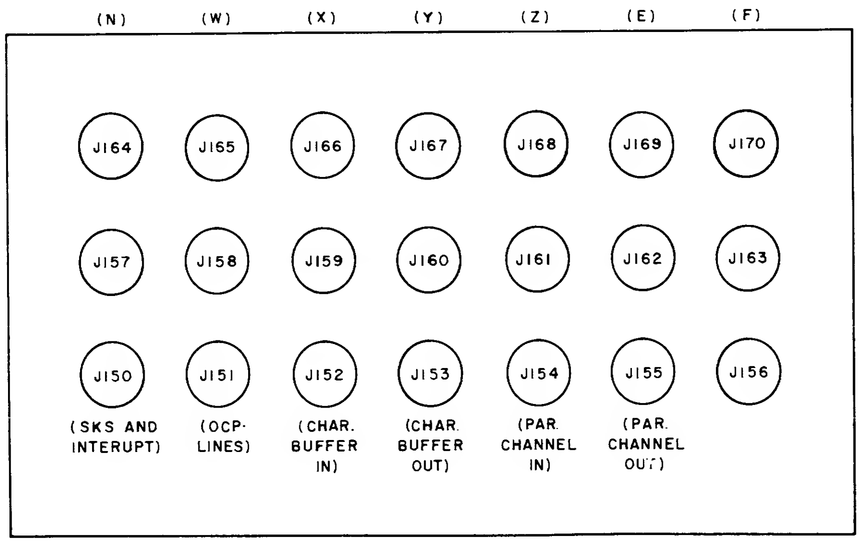


FIGURE 17—DDP-24 CONNECTOR PANEL

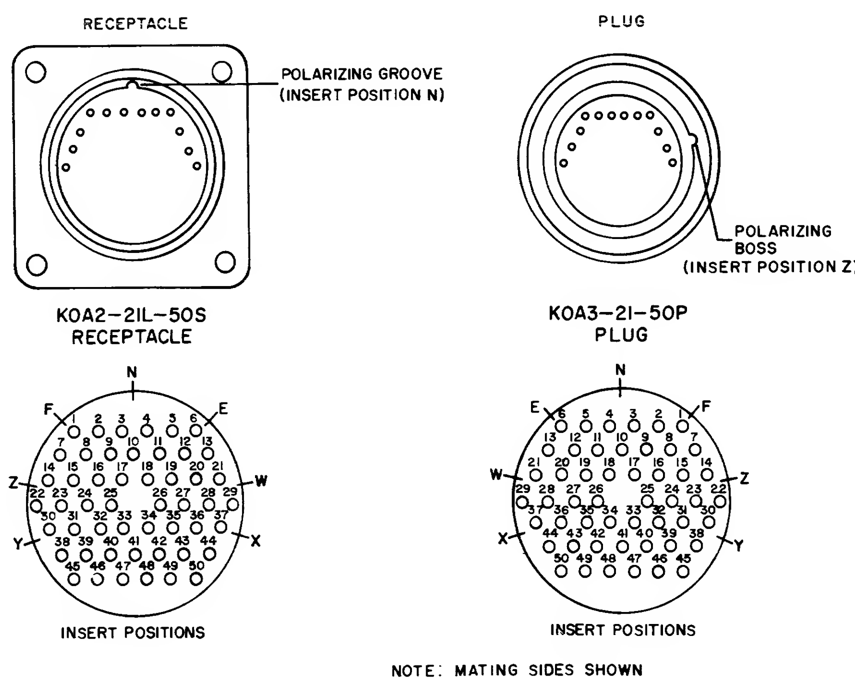


FIGURE 18—CONNECTOR POLARIZATION

TABLE 1
INTERNAL DDP-24 CONNECTOR ASSIGNMENTS

	CONN NO.	MAJOR FUNCTION	J TYPE (Recept)	P TYPE (Plug)	MAKE
Memories	J100A-D	AC pwr, mem 1-4	P302-AB	S-302-CCT	Cinch Jones
	J101A-D	DC pwr, mem 1-4	P312-DB	S-312-DB	Cinch Jones
	J103A-D	Sig lines mem 1-4	DD50S	DD50P	Cannon
	J106A-D	Sig lines mem 1-4	DD50S	DD50P	Cannon
	J102A-B	Fully buffered mem 1-2	DD50S	DD50P	Cannon
	J105A-B	Fully buffered mem 1-2	DD50S	DD50P	Cannon
AC Panel	J108	25 VAC to control panel	(126-198)	(126-195)	Amphenol
Power Supply	J109	−24 VDC and ind voltages	NK-27-32S	NK-27-21C 1/2	Cannon
Control Panel	J110	Indicator and switch signals	DD50P	DD50S	Cannon
Control Panel	J111	Indicator and switch signals	DD50P	DD50S	
Control Panel	J112	Indicator and switch signals	DD50P	DD50S	
Control Panel	J113	Indicator and switch signals	DD50P	DD50S	
Paper Tape Punch	J114	Voltages and signals	—	25034-16S	Continental
Typewriter	J115	Voltages and signals	—	MRA 50S+	Winchester
Paper Tape Reader	J116	Voltages and signals	—	UPCC-F2HSL-23	US Components

NOTE: J117 through J149 have been reserved for other internal DDP connectors when needed.

TABLE 2
EXTERNAL DDP-24 CONNECTOR ASSIGNMENTS

UNIT	CONN NO.	MAJOR FUNCTION	J TYPE	P TYPE	KEYWAY
Standard DDP	J150	SKS and interrupt	KOA2-21L-50S	KOA3-21-50P	Key (N)
	J151	OCP Lines	KOA2-21L-50S	KOA3-21-50P	Key (W)
	J152	Character buffer in	KOA2-21L-50S	KOA3-21-50P	Key (X)
	J153	Character buffer out	KOA2-21L-50S	KOA3-21-50P	Key (Y)
	J154	Parallel chan in	KOA2-21L-50S	KOA3-21-50P	Key (Z)
	J155	Parallel chan out	KOA2-21L-50S	KOA3-21-50P	Key (E)
Options	J156	Option	KOA2-21L-50S	KOA3-21-50P	Key (F)
	J157	Option	KOA2-21L-50S	KOA3-21-50P	Key (N)
	J158	Option	KOA2-21L-50S	KOA3-21-50P	Key (W)

TABLE 3

PIN ASSIGNMENTS FOR J150-SKS AND INTERRUPT

FUNCTION	PIN NO.	FUNCTION	PIN NO.
SKS20000	1	$\overline{\text{SKS30004}}$	26
$\overline{\text{SKS20000}}$	2	SKS30005	27
SKS20001	3	$\overline{\text{SKS30005}}$	28
$\overline{\text{SKS20001}}$	4	SKS30006	29
SKS20002	5	$\overline{\text{SKS30006}}$	30
$\overline{\text{SKS20002}}$	6	SKS30007	31
SKS20003	7	$\overline{\text{SKS30007}}$	32
$\overline{\text{SKS20003}}$	8		33
SKS20004	9	LO	34
$\overline{\text{SKS20004}}$	10	LI	35
SKS20005	11	L2	36
$\overline{\text{SKS20005}}$	12	L3	37
SKS20006	13	RTI-2	38
$\overline{\text{SKS20006}}$	14	RTI-3	39
SKS20007	15		40
$\overline{\text{SKS20007}}$	16	GRD	41
SKS30000	17		42
$\overline{\text{SKS30000}}$	18		43
SKS30001	19		44
$\overline{\text{SKS30001}}$	20		45
SKS30002	21		46
$\overline{\text{SKS30002}}$	22	GRD	47
SKS30003	23	GRD	48
$\overline{\text{SKS30003}}$	24		49
SKS30004	25		50

TABLE 4

PIN ASSIGNMENTS FOR J151-OCP

FUNCTION	PIN NO.	FUNCTION	PIN NO.
OCPx1001	1	OCPx1007	7
OCPx1002	2	OCPx1010	8
OCPx1003	3	GRD	41
OCPx1004	4	GRD	47
OCPx1005	5	GRD	48
OCPx1006	6		

TABLE 5

PIN ASSIGNMENTS FOR J152—CHARACTER BUFFER IN

FUNCTION	PIN NO.	FUNCTION	PIN NO.
EXD-1	1	Input drop-in pulse	30
EXD-2	2	Input device select	31
EXD-3	3	Channel busy	32
EXD-4	4	Stop signal	33
EXD-5	5	GRD	41
EXD-6	6	GRD	47
EXD-7	7	GRD	48

TABLE 6

PIN ASSIGNMENTS FOR J153—CHARACTER BUFFER OUT

FUNCTION	PIN NO.	FUNCTION	PIN NO.
K1	1	Output busy	30
K2	2	Output device select	31
K3	3	Channel busy	32
K4	4	Stop signal	33
K5	5	GRD	41
K6	6	GRD	47
K7	7	GRD	48

TABLE 7

PIN ASSIGNMENTS FOR J154—PARALLEL INPUT CHANNEL

FUNCTION	PIN NO.	FUNCTION	PIN NO.
Data 1	1	Data 17	17
Data 2	2	Data 18	18
Data 3	3	Data 19	19
Data 4	4	Data 20	20
Data 5	5	Data 21	21
Data 6	6	Data 22	22
Data 7	7	Data 23	23
Data 8	8	Data 24	24
Data 9	9	Input drop in pulse	30
Data 10	10	Input device select	31
Data 11	11	Channel busy	32
Data 12	12	Stop Signal	33
Data 13	13	GRD	41
Data 14	14	GRD	47
Data 15	15	GRD	48
Data 16	16		

TABLE 8

PIN ASSIGNMENTS FOR J155—PARALLEL OUTPUT CHANNEL

FUNCTION	PIN NO.	FUNCTION	PIN NO.
Data 1	1	Data 17	17
Data 2	2	Data 18	18
Data 3	3	Data 19	19
Data 4	4	Data 20	20
Data 5	5	Data 21	21
Data 6	6	Data 22	22
Data 7	7	Data 23	23
Data 8	8	Data 24	24
Data 9	9	Output busy	30
Data 10	10	Output device select	31
Data 11	11	Channel busy	32
Data 12	12	Stop signal	33
Data 13	13	Output strobe pulse	34
Data 14	14	GRD	41
Data 15	15	GRD	47
Data 16	16	GRD	48

INTERFACE MANUAL

ERRATA SHEET

Technical changes to the DDP-24 General-Purpose Computer require that the associated Interface Manual be updated as noted below. To update your manual, enter the indicated corrections on the appropriate pages.

Page	Change
4	In the left-hand column under "Pulse Specifications," add the word "min" after the words "0.25 μsec."
10	Change the title of the signal specifications in the left-hand column to "SIGNAL SPECIFICATIONS BUFFERED CHANNELS."
11	Change the first sentence of second paragraph to "The standard and optional general-purpose sense lines are tested with an SKS instruction, selected according to its decoded address portion (bits 10 through 24)."
12	In the third line of the first paragraph, change the expression "10-15" to "10-24."
18	In the third line of the "WORD-FORMING BUFFER" paragraph, change "WFM" to "WFB."
20	Change the NOTE in the right-hand column to read "Two versions of the word-forming buffer are available. One may be attached to the optional DMA channel, the other to a 24-bit parallel input-output channel."
21	In the illustration of Figure 16, the DDP-24 connector panel should appear in the lower portion of bay 4 on all units with serial number of 113 and higher.
24	In the FUNCTION column of Table 3, change the function "RTI-2" to "RTI" and delete "RTI-3."
24	In the FUNCTION column of Table 4, change the first eight functions to read as follows: OCPX1010, OCPX1011, OCPX1012, OCPX1013, OCPX1014, OCPX1015, OCPX1016, OCPX1017.